REMARKS

This is intended as a full and complete response to the Office Action dated November 21, 2005, having a shortened statutory period for response set to expire on February 21, 2006. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-21 are pending in the application. Claims 1-21 remain pending following entry of this response. Claims 1, 12, 16, 17 and 19 have been amended. Applicant submits that the amendments do not introduce new matter.

Claim Objections

Claims 16-21 are objected to because of the formalities. Claims 16, 17 and 19 have been amended to dependent upon Claim 15. Applicant submits that these objections are no longer valid and respectfully requests withdrawal of these objections.

Claim Rejections - 35 U.S.C. § 103

Claims 1, 8-10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Rostoker et al.* U.S. Patent No. 5,832,279 (hereinafter *Rostoker*), in view of *Hewitt et al.* U.S. Patent No. 6,339,808 (hereinafter *Hewitt*).

The Examiner takes the position that

"Rostoker discloses:

- an abstraction layer comprising a first plurality of registers conforming to the specific interrupt architecture (Rostoker, column 5 line 66 - column 6 line 6, figures 1 and 2);
- an implementation dependent layer, disposed in communication between the abstraction layer and the one or more processors (figure 1 numeral 12), comprising a second plurality of registers which correspond to the first plurality of registers (figure 3, numeral 58), wherein the implementation dependent layer is configured to receive interrupts and forward received interrupts to the one or more processors (Rostoker, column 6 lines 24-31, figures 1-3).

Rostoker does not disclose: to read and write data to the second plurality of registers in response to interrupts processed through the one or more processors.

However, Hewitt discloses to read and write data to the second plurality of registers in response to interrupts processed through the one or more processors (Hewitt, column 7 lines 49-60, figure 2).
It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Hewitt into the system of Rostoker to provide a system where the registers are utilized in the processing of data during an interrupt process.
The modification would have been obvious because one having ordinary skill in the art would want to have a system where the registers are utilized in the processing of data during an interrupt process (Hewitt, column 7 lines 49-60, figure 2)."

Applicant respectfully traverses this rejection.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the third criteria.

Rostoker discloses an Advanced Programmable Interrupt Controller (APIC) system with high speed serial data bus which operates generally in accordance to a conventional APIC system. *Hewitt* discloses an APIC configuration having a bridge integrated circuit and host bus connected to a multiple processors. *Hewitt* also operates generally in accordance to a conventional APIC system. Both references disclose systems for one specific interrupt architecture (i.e., the APIC architecture). The references cited by the Examiner do not teach, show or suggest an apparatus for passing interrupts from one or more devices configured for a specific interrupt architecture to one or more processors not designed for the specific interrupt architecture as claimed.

Furthermore, the references cited by the Examiner, either alone or combined, do not teach, show or suggest an implementation dependent layer configured to receive interrupts and forward received interrupts to one or more processors which are not

designed for the specific interrupt architecture and to read and write data to a second plurality of registers in response to interrupts processed through the one or more processors.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Rostoker*, in view of *Hewitt*, in further view of *Burgess*, U.S. Patent No. 6,892,260. Applicant notes that the Burgess reference is cited by the Examiner in the Office Action but not listed in the Notice of References Cited (form PTO-892).

As discussed above, *Rostoker* and *Hewitt* fail to teach or suggest all the claim limitations. *Burgess* discloses a method for executing an interrupt in a semaphore locking system such as a data processing system utilizing PowerPC processors. The references cited by the Examiner, either alone or combined, do not teach, show or suggest an apparatus for passing interrupts from one or more devices configured for a specific interrupt architecture to one or more processors not designed for the specific interrupt architecture as claimed.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Allowable Subject Matter

Claims 2-7 and 13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

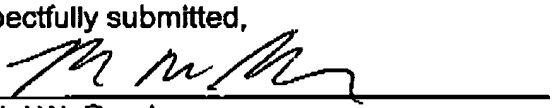
Applicant respectfully submits that the Office Action did not state any rejections under 35 U.S.C. 112. The claims are believed to be allowable in their present state as discussed above.

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the office action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted,



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